CPU-2 Z80 CPU BOARD

FEATURES:

* Z80 PROCESSOR
* ON BOARD ROM
* POWER ON JUMP TO ANY 256TH BIT. DIP SWITCH SELECTABLE HARDWARE GENERATION
* MAJOR EMPHASIS ON PROPER TIMING
* WILL WORK ON EXTENDER AT 4MHZ
* SWITCH SELECTABLE FOR 2/4MHZ OPERATION

C 1981, MIKOS ENGINEERING

QUANTITY	SCHEMATIC NAME	DESCRIPTION
2	U13,27	74LS00
4	U1,5,7,20	74LS02
2	U14,26	74LS04
1	U9	74S04
1	U25	74LS08
1	U19	74LS13
1	U8	74LS32
3	U11,15,21	74LS74
1	U16	74LS85
1	U10	74LS123
1	U28	74LS125
1	U12	74LS138
1	U6	74LS193
8	U17,30,31,32,33,34,35 36,	74LS244
2	U2,29	74LS367
2	U3,18	74LS368
1	U22	Z80A (4MHz)
2	VR1,VR2	7805/340T-5
1	U4	2716/2732
2	U23,24	spare
1	C3	10pf
1	C24	100pf
1	C12	.0033uf
18	C1,2,4-14,17-21	.1uf
4	C15,16,22,23	22uf tantalum
1	C25	33uf tantalum
3	R7,12,14	4.7K x 7 SIP pack
2	R5,6	560 ohm ¼w 5%
1	R8	10K ¼w 5%
1	R11	220 ohm ¼w 5%
1	R17	15K ¼w 5%
22	R1-4,9,10,13,15,16, 18-29,30	2.7K ¼w 5%
2	SW1,SW2	8 position DIP switch
1	Y1	16MHz Xtal
2		#361 heat sinks
9		16 pin sockets
8		20 pin sockets
1		40 pin sockets
16		14 pin sockets
18		wire wrap pins
2		sets #4-40 hardware

INTRODUCTION

The WAMECO CPU-2 is a Z-80 microprocessor based computer board for the S-100 bus. Many options have been included so the user is able to tailor the board for the required system configuration. Most of the S-100 bus signals have been provided. The Exceptions are; Interrupt, Enable, Stack and the CPU status signals on the data bus during the active state of PSYNC. The CPU-2 is designed to bring the power of the Z-80 microprocessor to an 8080 S-100 system.

2.0

2.1 2/4MHz Operation

The CPU-2 has provisions for operating with a 2MHz (standard) or 4MHz clock. For 2MHz operation the following jumper options must be selected.

a) connect E15 to E14
b) make R8 equal to a 10K ¼w, 5% resistor
c) make C12 equal to a .0033uf disc ceramic

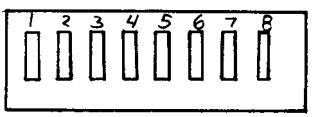
For operation at 4MHz (250ns cycle time), the following jumper options must be selected.

a) connect E13 to E14
b) make R8 equal to a 4.7K resistor
c) make C2 equal to a .001 uf disc ceramic

When operating at 4MHz insure that memory with an access time of 250ns or less is available, otherwise, add the required wait state for slower memories.

2.2 Power-up Jump

The CPU-2 has a power-on jump feature which, when the power is turned on (or system RESET occurs), forces an automatic jump to one of the 256 locations in memory. The memory boundries are in 256 block increments and are selected by dip switch SW2.



msb lsb

SW2

1	2	3	4	5	6	7	8
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	1
Ø	Ø	Ø	Ø	Ø	Ø	1	Ø
¦	¦	¦	¦	¦	¦	¦	¦
1	1	1	1	1	1	1	1

JUMP ADDRESS
0000 HEX
0100 HEX
0200 HEX
¦¦¦¦
FF00 HEX

The power-on jump feature allows operation of the CPU-2 without a front panel controller. If a front panel is installed in the computer the power-on jump feature should be disabled.

Power-on jump enabled:

a) Jumper E11 to E12
b) Open E19-E20

Power-on jump disabled:

a) Jumper E19-E20
b) Open E11-E12

2.3 EPROM Enable

Provisions have been made for operation with an on board EPROM. The EPROM may be either a 2716 or a 2732. Also, a wait state may be inserted if operation at 4MHz is desired. The addressing of the 2716/2732 on-board EPROM is in 4K boundries by closing an appropriate switch on SW1. The following table depicts the switch settings.

Ø = Closed, 1 = Open

Switch Setting 1268	EPROM address
0000	0000-0FFF
0001	1000-1FFF
0010	2000-2FFF
0011	3000-3FFF
0100	4000-4FFF
0101	5000-5FFF
0110	6000-6FFF
0111	7000-7FFF
1000	8000-8FFF
1001	9000-9FFF
1010	A000-AFFF
1011	B000-BFFF
1100	C000-CFFF
1101	D000-DFFF
1110	E000-EFFF
1111	F000-FFFF

Switches 3,4,5,7 are not used

To disable the on-board EPROM option:

Jumper E17-E18

For the 2716 EPROM option:

Jumper E16-E17
Jumper E8-E9

For the 2732 EPROM option:

Jumper E16-E17
Jumper E9-E10

If wait states are required with the on-board EPROM:

Jumper E4-E5

To disable the wait state operation: (normal mode)

Jumper E3-E5

The Power-up Jump and the on-board EPROM may be used together to provide a system boot-up.

2.4 MEM-WRITE Option

For systems that require operation without a front panel a memory write function must be supplied. The CPU-2 has provisions for generation the S-100 bus MWRITE function. To enable the MWRITE function connect the following:

Jumper E6-E7

otherwise leave E6-E7 open.

2.5 Front Panel Operation

The CPU-2 has provisions for connection to S-100 front panels. A 16 pin dip socket (J1) is available with the following pin designations:

(J1) DATA	PIN BUS	1,16 DØ	2,15 D1	3,14 D2
(J1) DATA	PIN BUS	4,13 D3	5,12 D4	6,11 D5
(J1) DATA	PIN BUS	7,10 D6	8,9 D7	

For WAMECO and IMSAI front panels a 16-pin ribbon cable assembly is all that is required.

3.0 THEORY OF OPERATION

3.1 Clock Generation

a) U9,Y1,R5,R6,C2 form an ocillator at 16MHz with buffering
b) U15 and U21 form a 2N Johnson counter to generate 01 and 02 bus signals
c) U29 provides the required drive for the S-100 bus.

3.2 Address Bus

a) U30,32 isolate the Z80 from the S-100 bus and also provide the necessary drive current
b) U31,8 are enabled during an I/O instruction and from address mirror A0-A7=A8-A15 on the address bus
c) the the address may be disabled thru U26 from ADDR DSBL

3.3 Data Bus

a) The data bus out is buffered to the S-100 bus by U34
b) The data bus in is buffered from the S-100 bus by U25. The data bus in buffer is disabled by one of the following conditions:

1 $\overline{SSW}$ $\overline{DSBL}$
2 single step, run (front panel operation)
3 $\overline{PDBIN}$, $\overline{SHLTA}$
4 on-board EPROM enable (if addressed)
5 on-board vector jump (if enabled)

3.4 Processor Status

(•) = AND, (+) = OR

a) SW0=RD • ($\overline{MI}$ • $\overline{IORQ}$)
b) SOUT=$\overline{IORQ}$ • $\overline{WR}$
c) SMI=$\overline{MI}$
d) SINP=$\overline{IORQ}$ • $\overline{RD}$
e) SMEMR=$\overline{RD}$ • $\overline{MREQ}$
f) PDBIN=RD+($\overline{MI}$ • $\overline{IORQ}$
g PWR=$\overline{WR}$ (delayed)

3.5 PSYNC

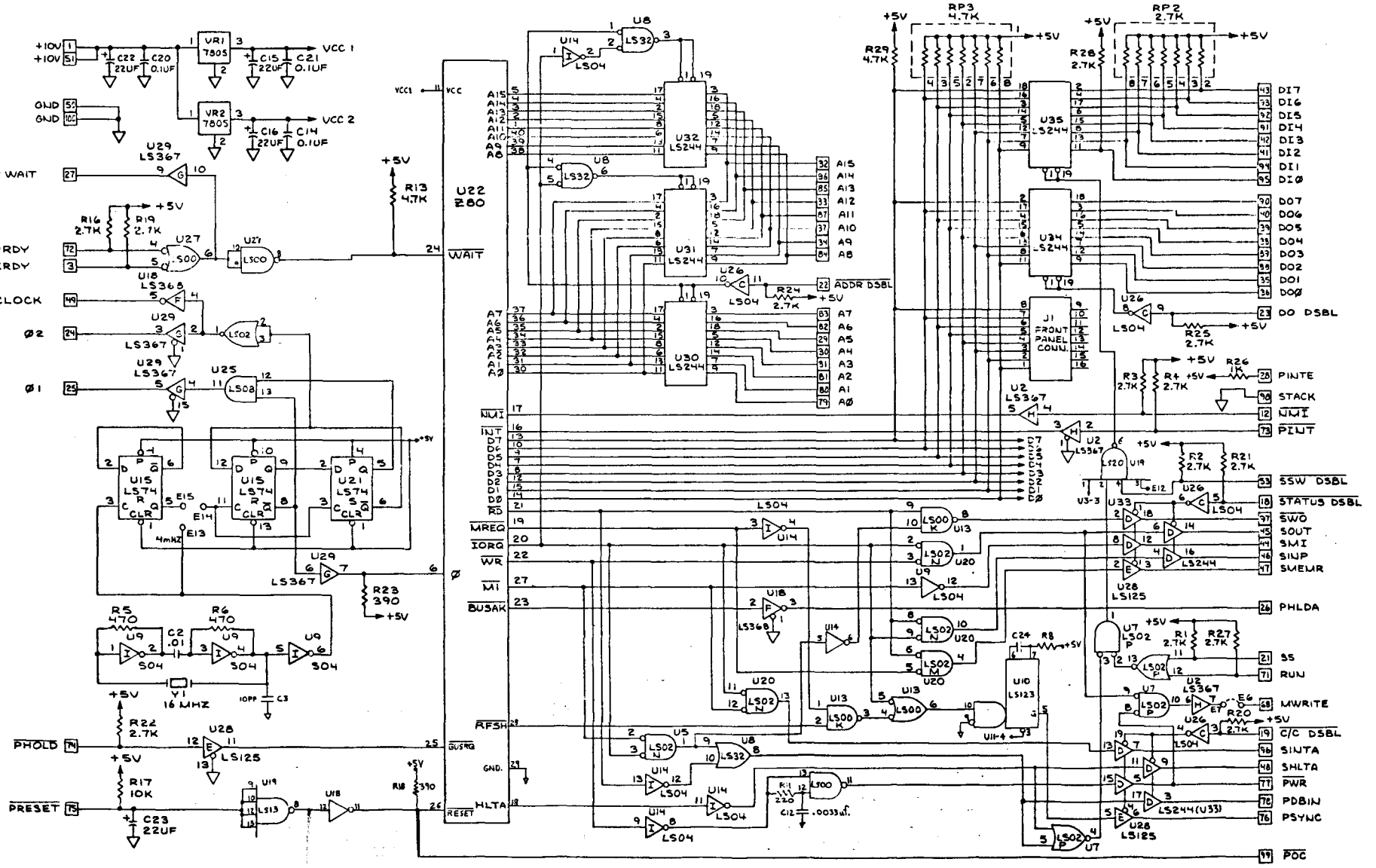
a) 500ns pulse @2MHz operation
b) 250ns pulse @4MHz operation
c) Pulse=(RFS•MREQ) + $\overline{IORQ}$
d) U13,14,10 & 28 provide the PSYNC signal to the S100 bus

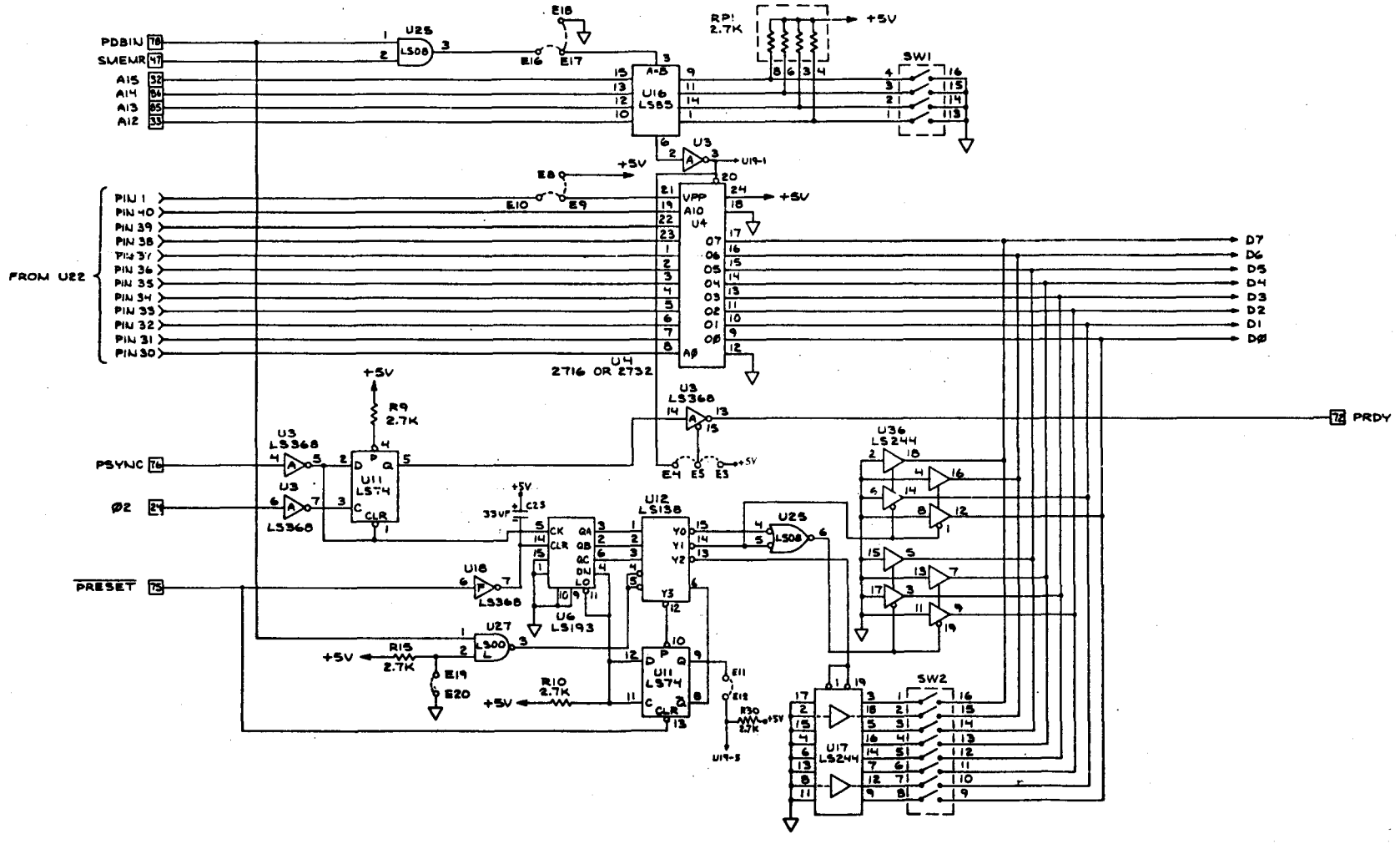
3.6 MWRITE

a) The on-board memory write function is generated by U20 ($\overline{SOUT}$), U9,7,2, and E6 through E7

3.7 EPROM ENABLE

a) U25,16,3 and E16-17 form a comparitor circuit that compares SW1 to address lines A12-A15. The output enable the chip select line on the EPROM (U4)


+10V
+10V
GND
GND
VR1 7805
VR2 7805
VCC 1
VCC 2
C22 22UF
C20 0.1UF
C15 22UF
C21 0.1UF
C16 22UF
C14 0.1UF
U22 Z80
VCC
GND
RESET
WAIT
BUSRQ
BUSAK
RFSH
HLTA
MREQ
IORQ
RD
WR
M1
INT
NMI
Φ
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
U29 LS367
P WAIT
PRDY
XRDY
R16 2.7K
R19 2.7K
U27 LS00
U27 LS00
R13 4.7K
U18 LS368
CLOCK
Ø2
Ø1
U25 LS08
U15 LS74
U21 LS74
4mHZ
R23 390
R5 470
R6 470
C2 .01
U9 S04
Y1 16 MHZ
10PF C3
PHOLD
PRESET
R22 2.7K
U28 LS125
R17 10K
C23 22UF
U19 LS13
R18 330
U8 LS32
U14 LS04
U32 LS244
U31 LS244
U30 LS244
U26 LS04
R24 2.7K
ADDR DSBL
U18 LS368
U20 LS02
U13 LS00
U5 LS02
U10 LS123
C24 R8
R11 220
C12 .0033uF
RP3 4.7K
RP2 2.7K
R29 4.7K
R28 2.7K
U35 LS244
U24 LS244
J1 FRONT PANEL CONN.
U2 LS367
R3 2.7K
R4 2.7K
R26 1K
R2 2.7K
R21 2.7K
U33 LS244
U28 LS125
R1 2.7K
R27 2.7K
R20 2.7K
U7 LS02
U2 LS367
R25 2.7K
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DOØ
DO DSBL
PINTE
STACK
NMI
PINT
SSW DSBL
STATUS DSBL
SWO
SOUT
SMI
SINP
SMEMR
PHLDA
SS
RUN
MWRITE
C/C DSBL
SINTA
SHLTA
PWR
PDBIN
PSYNC
POC


PDBIN 78
SMEMR 47
A15 32
A14 84
A13 85
A12 33
U25 LS08
E18
E16
E17
U16 LS85
RP1 2.7K
+5V
SW1
U3
U19-1
E8
E10
E9
FROM U22
PIN 1
PIN 40
PIN 39
PIN 38
PIN 37
PIN 36
PIN 35
PIN 34
PIN 33
PIN 32
PIN 31
PIN 30
U4 2716 OR 2732
VPP
A10
O7
O6
O5
O4
O3
O2
O1
O0
D7
D6
D5
D4
D3
D2
D1
D0
R9 2.7K
U3 LS368
PSYNC 74
Ø2 24
U11 LS74
C25 33UF
U12 LS138
U6 LS193
U18
PRESET 75
U27 LS00
R15 2.7K
E19
E20
R10 2.7K
E11
E12
R30 2.7K
U19-5
U25 LS08
U36 LS244
U17 LS244
SW2
72 PRDY

3.8 EPROM Wait States

a) U3,11 and E4-5 generate a 250ns wait state using PSYNC and Ø2 clock
b) the EPROM decoding must be valid before a wait cycle can be generated

3.9 On-Board Vector Jump

a) A vector jump is accomplished by jamming a jump instruction into the Z80 microprocessor
b) U6,11 and U12 generate the enables for three sets of drivers onto the bus
c) U36 generates the jump instruction (C3 Hex) and also the lower byte of the address
d) U17 and SW2 generate the upper byte of the jump address (one of the 256 locations
e) U27, E19-E20 and E11-E12 enable/disable the power-on vector jump option

4.0 GUARANTEE

The MIKOS ENGINEERING product you have purchased is guaranteed for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by MIKOS ENGINEERING, pre-paid freight, the board will be cheerfully replaced and shipping charges incurred by you will be repaid. The guaranty is limited to replacement of the board with an equivalent board, even though the board may be defective through negligence in manufacturing or through other fault.

For future reference, a print of the front and back traces of the CPU-2 is shown.

We sincerely hope that the CPU-2 will give you long and satisfactory service. If you have any problems with the CPU-2, or if you just want to comment on the board, please write me personally.

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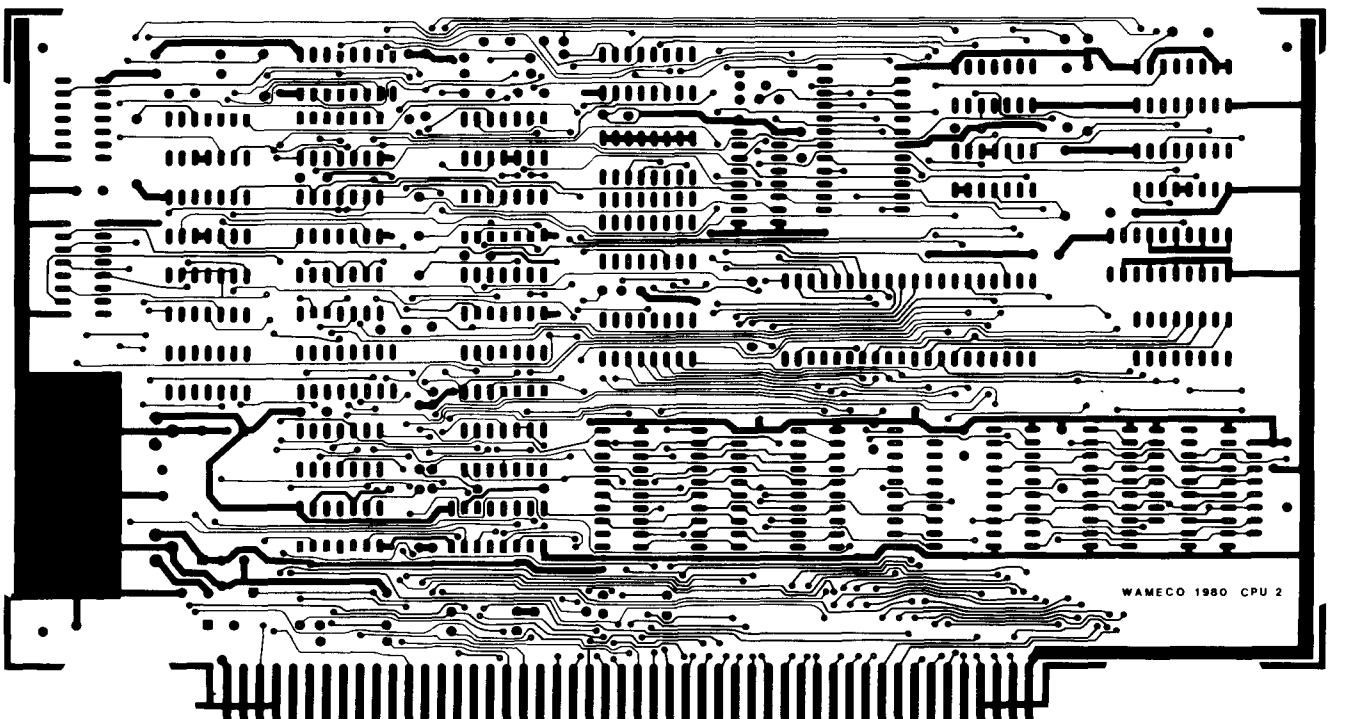
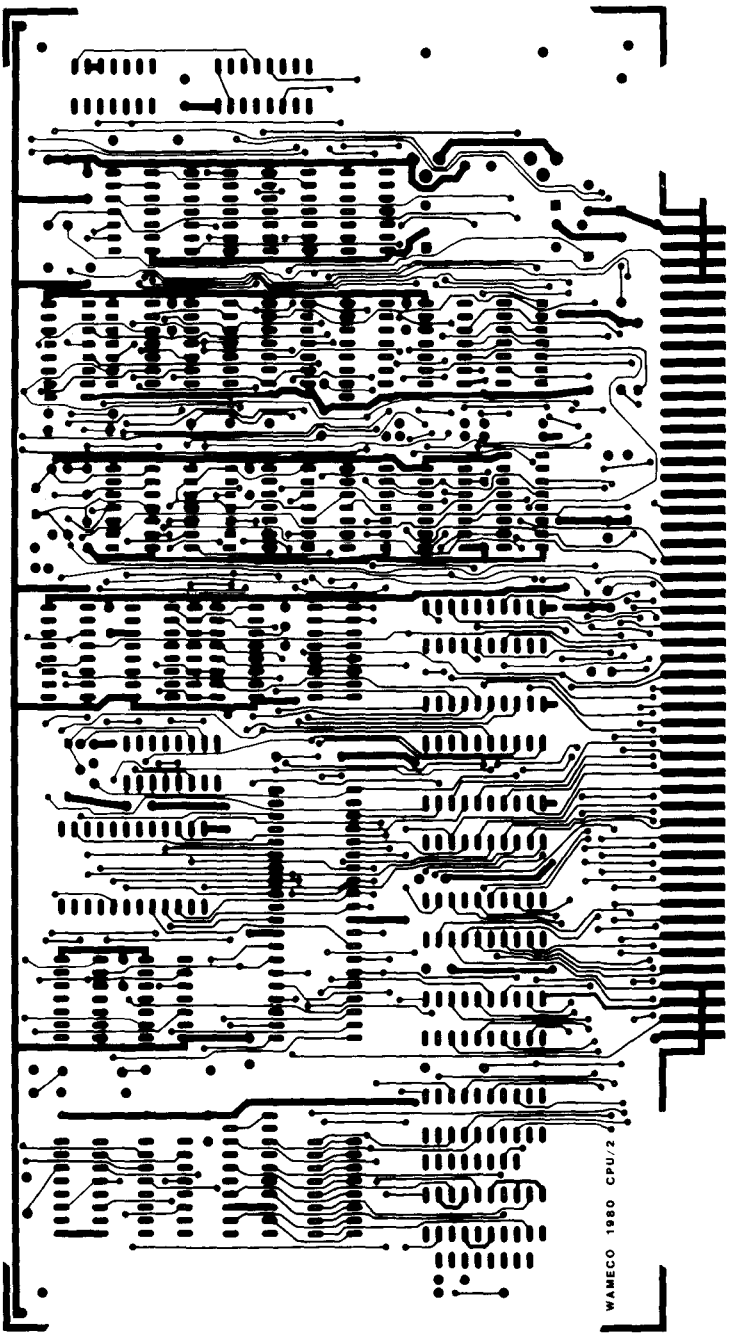
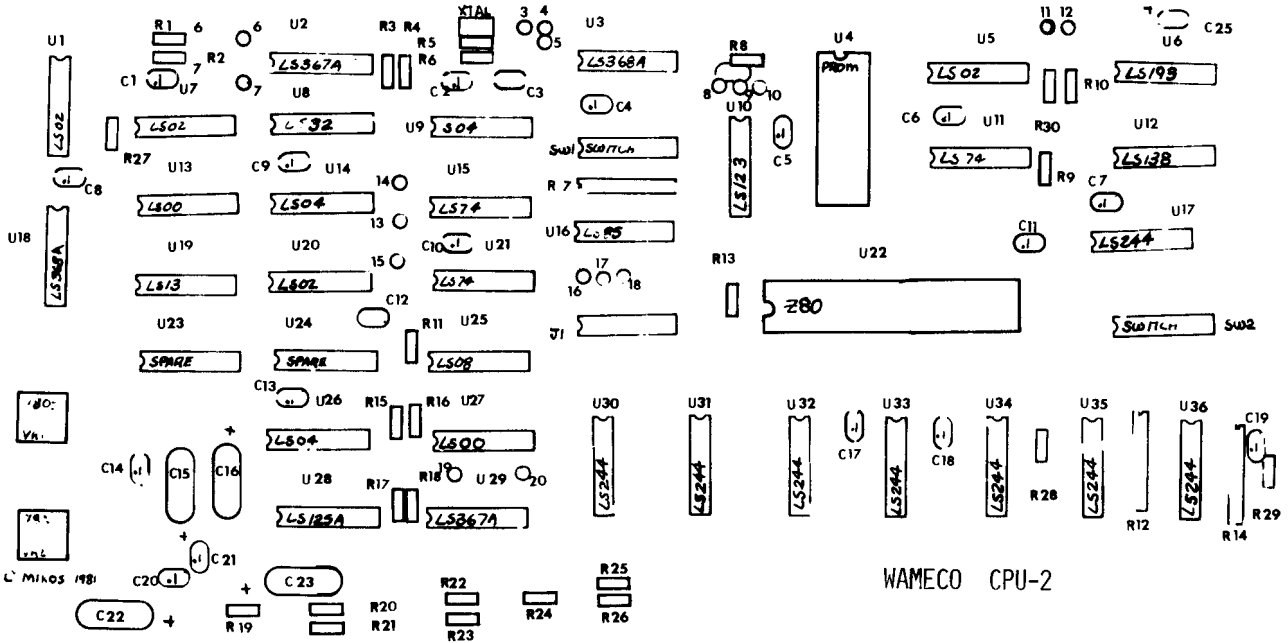

WAMECO 1980 CPU 2


WAMECO 1980 CPU/2


XTAL
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
J1
SW1
SW2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
C1
C2
C3
C4
C5
C6
C7
C8
C9
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C16
C17
C18
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C21
C22
C23
C25
LS02
LS367A
LS32
LS04
LS74
LS368A
LS00
LS13
LS08
SPARE
LS125A
LS123
PROM
LS74
LS138
LS244
Z80
SWITCH
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